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10/777,902	02/13/2004	Kenneth Koch II	10017912-3	6091

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,902	KOCH ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,8,9 and 11-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,8,9,11,14-19 and 22-24* is/are rejected.

7)☒ Claim(s) *6,12,13,20,22 and 26-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 26 and 27 are objected to because of the following informalities:

Claim 26, "and" should be deleted because it is already recited on line 35.

Claim 27 is objected to because it include the informality of claim 26.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 4, 8, 9, 11, 14 and 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohnishi (USP 5,633,600).

With respect to claim 1, Figure 1 of Ohnishi discloses a circuit, which includes: a first terminal (301) connected to a voltage (INPUT) having first and second levels and a transition between the level (see Figure 2); a driver (310, 311) including first (PFET 310) and second (NFET 311) opposite type transistors; opposite power supply terminals (Vdd, ground); an output terminal (OUTPUT 312); circuitry (302-309) connected between the first terminal (301) and the control electrodes (gates of 310 and 311), wherein the circuitry including at least one voltage responsive switchable capacitor (308 and/or 309, note that each of these capacitors 308 and 309 are responsive to the voltages at the gate of transistors 310 and 311, respectively, so that the capacitor is charged or discharge, and note that the capacitor is considered to be switchable

because it is switched between changed and discharge, and the threshold voltage is the voltage that causes the capacitor to change from charging to discharging and vice versa) which meets all the functional operations recited in the claims (line 30 of Col. 1 to line 27 of Col. 2).

With respect to claim 3, Figure 1 shows the at least one switchable capacitor is connected between one of the control electrodes and a DC power supply terminal (308 is connected between gate of 310 and VDD, and 309 is connected between gate of 311 and ground).

With respect to claim 4, Figure 1 shows the circuitry further includes a resistive element (304 or 305).

With respect to claim 8, Figure 1 shows the at least one switchable capacitor (308, 309) includes first and second voltage controllable switchable capacitors (308 and 309).

With respect to claim 9, Figure 1 shows the first capacitor 308 is connected between gate of 310 and VDD, and the second capacitor 309 is connected between gate of 311 and ground. Note that the functional recitations regarding the capacitors are also met because the capacitors in Figure 1 are connected between the respective control electrode of the first/second transistors and Vdd/ground as similar as applicant's invention, so the capacitors 308 and 309 in Figure 3 must also operates similarly.

With respect to claim 11, Figure 1 shows the circuitry further includes a first resistive element (304) and a second resistive element (305).

With respect to claim 14, Figure 1 shows the circuitry further includes first and second inverters (302 and 303) connected as recited in the claim.

With respect to the method claims 22-24, Figure 1 discloses a circuit which meets all the limitations of the apparatus claims as discussed above. Hence, the operations of the circuit in

Figure 1 also deems to meet all the method steps as recited in claims 22-24. Note that the switch-off of a capacitor is interpreted as the capacitor is "discharged", and the switch-on is "charged".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi (USP 5,633,600) in view of Wanlass (USP 3,356,858), and further in view of in view of Vikinski (USP 6,150,862).

With respect to claim 15, the circuit in Figure 1 of Ohnishi meets all the limitations of this claim except for specifically discloses that each of the inverters (302, 303) comprises field effect transistors. However, the Wanlass reference discloses in Figure 5 that a CMOS inverter is easily formed by using a PMOS transistor connected with an NMOS transistor, wherein the CMOS inverter provides advantage such as low power consumption. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 1 of Ohnishi by using CMOS inverter having a PMOS and an NMOS as taught in Figure 5 of Wanlass for each of the inverters 303 and 303 (Figure 1, Ohnishi) for the purpose of reduce power consumption.

The above modification/combination (Ohnishi in view of Wanlass) meets all the limitations of claim 15 except that the first and second capacitors comprise field effect

transistors. However, the Vikinski reference discloses that a capacitor is easily integrated by using a field effect transistor that has its drain and its source connected together (see the two capacitors in 220 in Figure 2 of Vikinski). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the above combination/modification (Ohnishi and Wanlass) to use specific transistor-connected-capacitors (as taught by Vikinski) for broad capacitor elements 308 and 309 in Figure 1 of Ohnishi for the purpose of easily integrated the circuit, and it is old and well known that integrated capacitor (i.e., transistor-connected-capacitor) occupies less space on a chip. Thus, this modification/combination meets the limitations of claim 15 that the first and second transistors are FETs, the first and second inverters comprise FETs, and the first and second capacitors comprise FETs.

With respect claim 16, it is seen from the modification/combination as discussed in claim 15 above that all the FETs are included in an integrated circuit chip including the first and second resistors (304, 305, Figure 1 of Ohnishi) respectively connected to the FETs of the first and second transistors and connected with the first and second inverters.

With respect to claim 17, from Figure 1 of Ohnishi, by broadly reading first inverter as (combined of elements 302 and 304, i.e., the input of the first inverter is input of 302 and the output of the inverter is the terminal of 304 that connected directly to gate of 310), and second inverter (combined of elements 303 and 305, i.e., the input of the second inverter is input of 303 and the output of the inverter is the terminal of 305 that connected directly to gate of 311), then the first and second resistors (304 and 305) are included in the first (302, 304) and second (303, 305) inverters.

With respect to claim 18, this claim is rejected for the same manner as discussed in claim 17 above.

With respect to claim 19, it is seen from the above combination/modification (discussed in claim 17) that the first resistor (304) is connected between the source-drain path of the NFET of the first inverter and the output terminal of the first inverter (i.e., between the source-drain path of the NFET inside 302 and the gate of transistor 310), and the second resistor (305) is connected between the source-drain path of the PFET of the second inverter and the output terminal of the second inverter (i.e., between the source-drain path of the PFET inside 303 and the gate of transistor 311).

Allowable Subject Matter

6. Claims 26 and 27 would be allowed if amended to overcome the minor informalities set forth above.

7. Claims 6, 12, 13, 20, 22, and 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome the indefiniteness and informalities set forth above.

Responses to Arguments

8. Applicant's arguments filed on 1/30/07 have been fully considered but they are not persuasive.

Applicant argues that capacitors 308 and 309 of Ohnishi are not switched from an initial finite capacitance value to a substantially open circuit as required in claim 1. However, this argument is not persuasive because when voltage at the input 301 transition from Vdd (Hi) to

ground (Lo), then the voltage at the gate of transistor 310 would be from ground (Lo) to Vdd. Therefore, initially when gate of 310 is at ground then the voltage across capacitor 308 is Vdd and thus the capacitor 308 is fully charged and thus capacitor 308 will have an initial finite value; and while the voltage at the gate of 310 is changing from ground toward Vdd, and the voltage across capacitor 308 will be decreasing and when the voltage at the gate of 310 is greater than a predetermined voltage (the voltage at which the capacitor 308 is switched from charging to discharging) then the capacitor 308 will be discharged and thus the capacitor 308 will functions as an open circuit. Similarly, when then voltage of gate 311 is at Vdd then the capacitor 309 will have an initial capacitance value, and while the gate 309 is changing from Vdd toward ground, and when voltage 311 is less than a predetermined voltage (voltage at which capacitor is changing from charged to discharged) then capacitor 309 will functions as an open circuit. Note that the operation of capacitors 308 and 309 is substantially as the operation of capacitors 34 and 32, respectively, of applicant's invention.

Applicant further argues that claim 222 distinguishes over Figure 1 of Ohnishi by requiring first and second capacitors to be switched off and remained switched or turned off, and capacitors 308 and 309 are not switched or turned off; instead, the capacitors have constant values throughout their operation. However, this argument is not persuasive because as discussed above the capacitances of capacitors 308 and 309 of Ohnishi are changing between charging and discharging, and when the capacitors are fully discharged, the capacitors are switched off.

For claim 9, applicant argues that the capacitors of Ohnishi are not substantially open circuits as function of thresholds, and capacitors 308 and 309 are always have the same value

and are not switched to an open circuit condition. However, this argument is not persuasive because capacitors 308 and 309 are switched from initial capacitance value to an open-circuit condition as discussed above (see the response to arguments above for more detail of discussion the operation of capacitors 308 and 309).

For claim 19, applicant argues that the resistors 304 and 305 are connected to terminal outsides of inverters 302 and 303, and thus there are no connections of resistors 304 and 305 between output terminals of inverters 302 and 303 and transistors that are part of the inverters. However, this argument is not persuasive because, as clearly discussed in the rejection of claim 17, the first inverter is the combined of elements 302 and 304 (i.e., the input of the first inverter is input of 302 and the output of the inverter is the terminal of 304 that connected directly to gate of 310), and second inverter is the combined of elements 303 and 305 (i.e., the input of the second inverter is input of 303 and the output of the inverter is the terminal of 305 that connected directly to gate of 311), then the first and second resistors (304 and 305) are included in the first (302, 304) and second (303, 305) inverters. Thus, each of the resistors 304 and 305 is connected between the output terminal of the respective inverter and the transistor that is part of the respective inverter. Note that the rejection of claim 19 clearly discussed that the first resistor (304) is connected between the source-drain path of the NFET of the first inverter and the output terminal of the first inverter (i.e., between the source-drain path of the NFET inside 302 and the gate of transistor 310), and the second resistor (305) is connected between the source-drain path of the PFET of the second inverter and the output terminal of the second inverter (i.e., between the source-drain path of the PFET inside 303 and the gate of transistor 311).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER